Please add new claims 41-110 as follows:

--41. A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming an organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film; and

forming a pixel electrode over said organic leveling film through said opening,

wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion of said opening, and

wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion.

42. A method according to claim 41 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

43. A method according to claim 41 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

44. A method according to claim 41 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

45. A method according to claim 41 wherein said gate electrode comprises aluminum.

46. A method according to claim 41 wherein said gate insulating film comprises silicon oxide.

47. A method according to claim 41 wherein said amorphous semiconductor film is deposited through plasma CVD.

48. A method according to claim 41 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

49. A method according to claim 41 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

50. A method according to claim 41 wherein said pixel electrode extends over said channel region.

51. A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

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patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a color filter over a second substrate;

forming a second organic leveling film over said color filter;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other.

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52. A method according to claim 51 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

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53. A method according to claim 51 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

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54. A method according to claim 51 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

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55. A method according to claim 51 wherein said gate electrode comprises aluminum.

16 11
56. A method according to claim 51 wherein said gate insulating film comprises silicon oxide.

57. A method according to claim 51 wherein said amorphous semiconductor film is deposited through plasma CVD.

58. A method according to claim 51 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

59. A method according to claim 51 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

60. A method according to claim 51 wherein said pixel electrode extends over said channel region.

61. A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a resin black matrix over a second substrate;

forming a second organic leveling film over said resin black matrix;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and

said pixel electrode are opposed to each other.

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62. A method according to claim 61 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

63. A method according to claim 61 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

64. A method according to claim 61 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

65. A method according to claim 61 wherein said gate electrode comprises aluminum.

66. A method according to claim 61 wherein said gate insulating film comprises silicon oxide.

67. A method according to claim 61 wherein said amorphous semiconductor film is deposited through plasma CVD.

68. A method according to claim 61 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

69. A method according to claim 61 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

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30. A method according to claim 21 wherein said pixel electrode extends over said channel region.

31. A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a color filter over a second substrate;

forming a resin black matrix over said second substrate;

forming a second organic leveling film over said color filter and said resin black matrix;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other.

32. A method according to claim 31 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

33. A method according to claim 31 further comprising a step of forming a pair of

impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

74. A method according to claim 71 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

75. A method according to claim 71 wherein said gate electrode comprises aluminum.

76. A method according to claim 71 wherein said gate insulating film comprises silicon oxide.

77. A method according to claim 71 wherein said amorphous semiconductor film is deposited through plasma CVD.

78. A method according to claim 71 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

79. A method according to claim 71 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

80. A method according to claim 71 wherein said pixel electrode extends over said channel region.

81. A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a color filter over a second substrate;

forming a second organic leveling film over said color filter;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other,

wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion of said opening, and

wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion.

82. A method according to claim 81 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

83. A method according to claim 81 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

84. A method according to claim 81 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

85. A method according to claim 81 wherein said gate electrode comprises aluminum.

86. A method according to claim 81 wherein said gate insulating film comprises silicon oxide.

87. A method according to claim 81 wherein said amorphous semiconductor film is deposited through plasma CVD.

88. A method according to claim 81 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

89. A method according to claim 81 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

90. A method according to claim 81 wherein said pixel electrode extends over said channel region.

91. A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a resin black matrix over a second substrate;

forming a second organic leveling film over said resin black matrix;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other,

wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion of said opening, and

wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion.

92. A method according to claim 91 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

93. A method according to claim 91 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

94. A method according to claim 91 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

95. A method according to claim 91 wherein said gate electrode comprises aluminum.

96. A method according to claim 91 wherein said gate insulating film comprises silicon oxide.

97. A method according to claim 91 wherein said amorphous semiconductor film is deposited through plasma CVD.

98. A method according to claim 91 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

99. A method according to claim 91 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

100. A method according to claim 91 wherein said pixel electrode extends over said channel region.

101. A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

forming a gate insulating film over said gate electrode;

depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

patterning said semiconductor film into an island comprising a channel region;

forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

forming an opening in said organic leveling film;

forming a pixel electrode over said organic leveling film through said opening;

forming a color filter over a second substrate;

forming a resin black matrix over said second substrate;

forming a second organic leveling film over said color filter and said resin black matrix;

forming a counter electrode on said second leveling film; and

facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other,

wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion of said opening, and

wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion.

102. A method according to claim 101 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

103. A method according to claim 101 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

104. A method according to claim 101 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

105. A method according to claim 101 wherein said gate electrode comprises

aluminum.

106. A method according to claim 101 wherein said gate insulating film comprises silicon oxide.

107. A method according to claim 101 wherein said amorphous semiconductor film is deposited through plasma CVD.

108. A method according to claim 101 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

109. A method according to claim 101 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

110. A method according to claim 101 wherein said pixel electrode extends over said channel region.--

REMARKS

The Examiner's Official Action dated August 31, 1999 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a One Month Extension of Time* which extends the shortened statutory period for response to December 21, 1999. Accordingly, applicant respectfully submits that this response is being timely filed.

Claims 21-40 were pending in the present application prior to the above amendment. Claims 21-40 have been canceled and new claims 41-110 have been added to recite additional protection to which applicant is entitled. Accordingly, new claims 41-110 are